

WE CLAIM:

1 1. An integrated circuit, comprising:

2 first power rails supporting a first voltage differential;

3 second power rails supporting a second voltage differential, wherein said second
4 voltage differential is smaller than said first voltage differential;

5 a plurality of second circuits outputting a second voltage swing, wherein said
6 second voltage swing is determined by said second voltage differential;

7 a plurality of signal lines, wherein said signal lines are driven by said second
8 voltage swing; and

9 a plurality of regeneration circuits, wherein said regeneration circuits are receiving
10 said second voltage swing and are outputting a first voltage swing, wherein said first
11 voltage swing is determined by said first voltage differential.

1 2. The integrated circuit of claim 1, wherein in said second circuits NFET and PFET
2 devices have low thresholds, wherein said low thresholds are lower than those thresholds
3 which pertain to the technology of said integrated circuit.

1 3. The integrated circuit of claim 2, wherein in said second circuits said low thresholds
2 are dynamically adjusted.

1 4. The integrated circuit of claim 1, wherein in said restoring circuits NFET and PFET
2 devices have custom thresholds, wherein said custom thresholds are derived from said
3 first and second voltage differentials.

1 5. The integrated circuit of claim 4, wherein in said restoring circuits said custom
2 thresholds are dynamically adjusted.

1 6. The integrated circuit of claim 1, wherein said integrated circuit is a DRAM, and said
2 signal lines comprise global bit-lines.

1 7. The integrated circuit of claim 6, wherein memory cells in said DRAM are written with
2 said first voltage swing.

1 8. The integrated circuit of claim 6, further comprising interface regeneration circuits,
2 wherein said interface regeneration circuits are receiving said second voltage swing and
3 are outputting an interfacing voltage swing, wherein said interfacing voltage swing is
4 larger than said second voltage swing, and wherein I/O operations in said DRAM are
5 performed with said interfacing voltage swing.

1 9. The integrated circuit of claim 6, wherein said DRAM has a single ended data-line
2 structure.

1 10. The integrated circuit of claim 9, wherein a Read and a subsequent WriteBack
2 operation occurs in one cycle, wherein said integrated circuit operates in cycles.

1 11. The integrated circuit of claim 9, wherein a Read and a subsequent WriteBack
2 operation occurs in more than one cycle, wherein said integrated circuit operates in
3 cycles.

1 12. The integrated circuit of claim 9, further comprising a single ended primary sense
2 amplifier with local storage and write-back capability.

1 13. The integrated circuit of claim 6, wherein said DRAM is an embedded DRAM macro.

1 14. A wide bandwidth memory, comprising:
2 simultaneously operable connection paths between a string of memory cells and
3 corresponding Input/Output terminals, wherein said string of memory cells are essentially
4 all the memory cells which are attached to the same wordline, wherein said wide
5 bandwidth memory has a plurality of wordlines and a plurality of memory cells; and
6 a single ended data-line structure.

1 15. The wide bandwidth memory of claim 14, further comprising:
2 first power rails supporting a first voltage differential;

1 second power rails supporting a second voltage differential, wherein said second
2 voltage differential is smaller than said first voltage differential;

3 a plurality of second circuits outputting a second voltage swing, wherein said
4 second voltage swing is determined by said second voltage differential;

5 a plurality of signal lines, wherein said signal lines are driven by said second
6 voltage swing; and

7 a plurality of regeneration circuits, wherein said regeneration circuits are receiving
8 said second voltage swing and are outputting a first voltage swing, wherein said first
9 voltage swing is determined by said first voltage differential.

1 16. The wide bandwidth memory of claim 14, wherein said wide bandwidth memory is a
2 DRAM.

1 17. The wide bandwidth memory of claim 16, further comprising a single ended primary
2 sense amplifier with local storage and write-back capability.

1 18. A processor, comprising:

2 at least one embedded memory macro, wherein said at least one embedded
3 memory macro is further comprising:

4 first power rails supporting a first voltage differential;

5 second power rails supporting a second voltage differential, wherein said

1 second voltage differential is smaller than said first voltage differential;

2 a plurality of second circuits outputting a second voltage swing, wherein
3 said second voltage swing is determined by said second voltage differential;

4 a plurality of signal lines, wherein said signal lines are driven by said
5 second voltage swing; and

6 a plurality of regeneration circuits, wherein said regeneration circuits are
7 receiving said second voltage swing and are outputting a first voltage swing, wherein said
8 first voltage swing is determined by said first voltage differential.

1 19. The processor of claim 18, wherein said least one embedded memory macro has a
2 single ended data-line structure.

1 20. The processor of claim 18, wherein said least one embedded memory macro is an
2 embedded DRAM.

1 21. A method for conserving power in an integrated circuit, comprising the steps of:
2 providing said integrated circuit with power rails supporting a reduced voltage
3 differential, wherein said reduced voltage differential is smaller than a nominal voltage
4 differential of said integrated circuit; and
5 driving signal lines in said integrated circuit with a reduced voltage swing,
6 wherein said reduced voltage swing is determined by said reduced voltage differential.

- 1 22. The method of claim 21, wherein said integrated circuit is chosen to be an embedded
2 DRAM macro, and said signal lines are chosen to be global bit-lines.
- 1 23. The method of claim 22, wherein said embedded DRAM macro is chosen to have a
2 single ended data-line structure.